

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Houston	Docket No.: TI-28032
Serial No.: Divisional of 09/661,659	Examiner: TBD
Filed: Herewith	Art Unit: TBD
For: SEMICONDUCTOR DEVICE WITH FULLY SELF-ALIGNED LOCAL INTERCONNECTS, AND METHOD FOR FABRICATING THE DEVICE	

Preliminary Amendment

Assistant Commissioner of Patents
Washington, DC 20231

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)

I hereby certify that this correspondence is being deposited with the
U.S. Postal Service as First Class Mail in an envelope addressed to:
Assistant Commissioner for Patents, Washington, D.C. 20231 on

2-27-02

Marianna Smith
Marianna Smith

Dear Sir:

Please enter the following amendments prior to examination of the instant application.

In the Specification:

Please amend the specification by inserting before the first line the sentence:

--This is a divisional application of Serial No. 09/661,659 filed 09/14/00, which is a non-provisional application claiming priority of provisional application number 60/161,651 filed 10/20/99.--

In the Claims:

Please cancel Claims 1-17.

Please add the following new claims:

-- 23. An integrated circuit including a transistor, said transistor comprising:

a control terminal extending above a plane of semiconductor material, said control terminal having two side portions and a top portion covered by an insulating layer; and

first and second terminals on either side of said control terminal, said first and second terminals extending above said plane of semiconductor material such that top portions of said first and second terminals are substantially coplanar with said insulating layer covering said top portion of said control terminal.

24. The circuit of Claim 23, wherein said insulating layer covering said top portion of said control terminal comprises alternating sub-layers of first and second insulating materials.

25. The circuit of Claim 24, wherein said first insulating material is silicon oxide and said second insulating material is silicon nitride.

26. The circuit of Claim 23, wherein said control terminal is a gate electrode of a field effect transistor and said first and second terminals comprise local interconnections to drain and source regions of said transistor.

27. An integrated circuit including a transistor, said transistor comprising:

a gate stack extending above a plane of semiconductor material, said gate stack comprising a gate dielectric and a gate electrode over said gate dielectric, said gate electrode comprising side and top portions covered by insulating material; and

local interconnection terminals on opposing sides of said gate stack and abutting said insulating material on said side portions of said gate electrode, said local interconnection terminals extending above said plane of semiconductor

material such that top portions of said local interconnection terminals are substantially coplanar with said insulating material covering said top portion of said gate electrode.

28. The circuit of Claim 27, wherein said insulating material covering said top portion of said control terminal comprises alternating layers of first and second insulating materials.

29. The circuit of Claim 28, wherein said first insulating material is silicon oxide and said second insulating material is silicon nitride.

30. The circuit of Claim 27, wherein each of said local interconnection terminals includes a column of insulating material. —

Claims 18-30 are now pending in this Application. Applicant respectfully requests entry and consideration of these claims.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,



Michael K. Skrehot
Reg. No. 36,682

Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, TX 75265
PHONE: 972 917-5653
FAX: 972 917-4418